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MANAGED BY UT-BATTELLE FOR THE DEPARTMENT OF ENERGY

CuRIE Interconnect Technology for Improved Energy Efficiency in IC Chips

ARPA-E Technology Innovation Showcase, Washington D.C.
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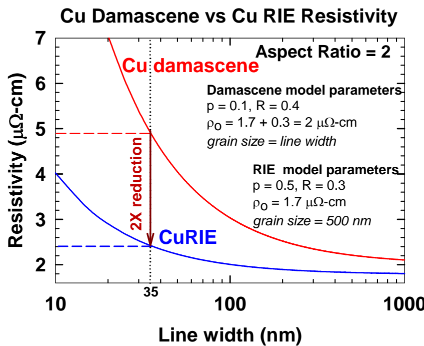
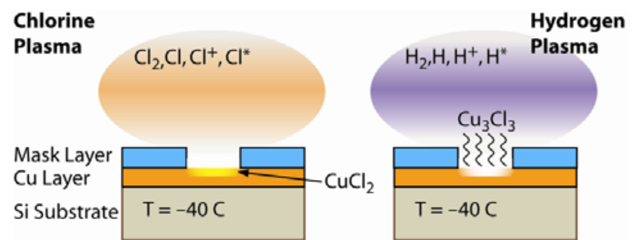
Abstract

This project aims to develop copper reactive ion etching (CuRIE) technology for manufacturing nanoscale copper interconnects used in IC chips in order to achieve a 50% reduction in the electrical resistivity of sub-50 nm wide copper nanowires and a potential energy savings of over $30 Billion/year. This new approach is demanded by the exponentially increasing resistivity with shrinking feature sizes of copper interconnects manufactured with current damascene technology. Furthermore, the environmental footprint associated with current interconnect manufacturing is also expected to be significantly reduced with the proposed CuRIE technology.

Technology Benefit: ***Minimizing "Size Effects"***

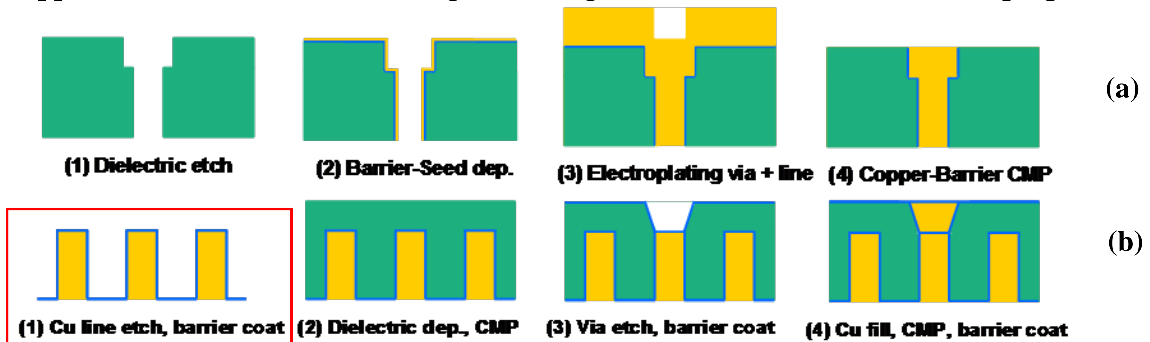


Transformational technology:
Low temperature plasma etching of copper



Top Left: *Electrical resistivity as a function of feature width for Cu damascene and CuRIE manufactured interconnects. Suitable parameters in the Fuchs-Sondheimer/Mayadas-Shatzkes models were utilized to generate the plots above.* ***Top Right:*** *Proposed 2-step low temperature reactive ion (RIE) or plasma etching process for copper (Kulkarni and DeHoff, J. Electrochemical Society, 2002; US Patent 7064076, 2006; Wu, Levitin and Hess, J. Electrochemical Society, 2010).*

Copper Interconnect Manufacturing Technologies: Dual-damascene vs CuRIE (proposed)



(a) Simplified Cu dual-damascene process (top) and (b) proposed CuRIE process (bottom). In the damascene process after dielectric line and via etch (1a), a barrier (TaN/Ta) and Cu seed layer is vapor deposited (2a), Cu is electroplated (3a), and excess Cu is removed using chemical mechanical planarization (CMP) (4a); in the subtractive process, a blanket Cu film is plasma etched and a barrier is deposited (1b), dielectric is vapor deposited and excess dielectric is removed using CMP (2b), dielectric via is plasma etched and barrier is deposited (3b), Cu via is vapor deposited and excess Cu is removed using CMP (4b).

Benefits

Reduced power consumption in IC devices; hence potential energy savings of 300 Billion KWh/yr

Lower environmental impact of semiconductor manufacturing operations

Improved reliability and performance of IC devices.

Improved efficiency in design and manufacturing

Enable continued adherence to Moore's law

Industry Impact

$226 Billion global chip sales in 2009 (Semiconductor Industry Association http://www.sia-online.org)

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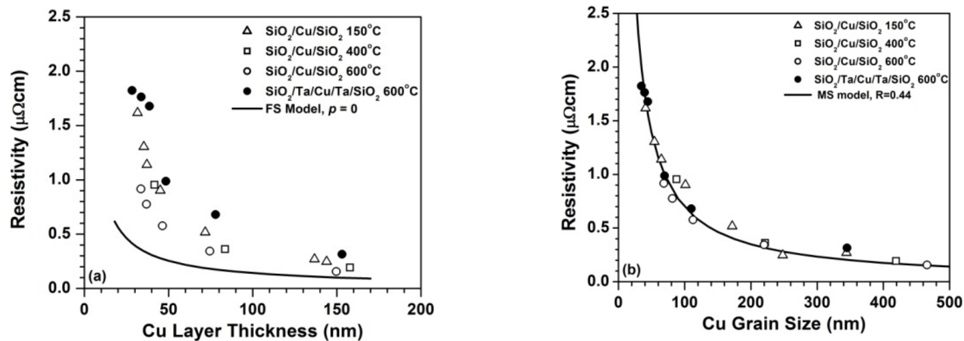
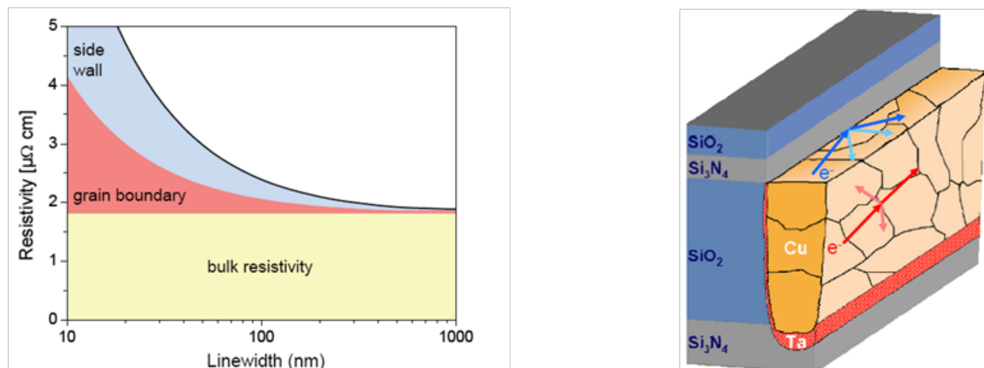
Scientific Basis - Understanding Electron Scattering: Electron scattering in copper nano films and wires is attributed to three primary factors: surface scattering, grain boundary scattering and impurity scattering. Fundamental work by ORNL and its collaborators has focused on understanding the relative contributions of these factors by conducting experimental studies in thin films, specific grain boundary resistivity measurements using a Four-probe Scanning Tunneling Microscope (STM), microstructure and first-principles grain boundary resistivity measurements and modeling.

A. Size Effects in Thin Films: Dominant role of grain boundary scattering in low-temperature resistivity of both SiO_2 and Ta/SiO_2 encapsulated Cu thin films demonstrated by the experimental variation and quantification of film thickness, roughness and grain size. Size of more than 18,000 grains from 21 films was measured from STEM dark field images.



Top Left:** Resistivity of SiO_2 and Ta/SiO_2 encapsulated and annealed Cu thin films as a function of film thickness. The solid curve is the prediction of the Fuchs-Sondheimer model for a maximum resistivity increase, having a specularity coefficient, p, equal to zero.* ***Top Right: *Resistivity of SiO_2 and Ta/SiO_2 encapsulated and annealed Cu films as a function of measured average grain size. The solid curve is the prediction of the Mayadas-Shatzkes model for a grain boundary reflection coefficient, R, equal to 0.44. (Sun, Barmak, Coffey et al., Phy. Rev. B, 2009).*

B. Size Effects in Damascene Nanowires: The most comprehensive study of size effects in the electrical resistivity of damascene copper was performed by Infineon and shows an approximate equal contribution from both surface (side-wall) and grain boundary scattering.



***Top Left:** Resistivity as a function of line width (ITRS 2007) for copper damascene (electroplated) wires. A fit to the resistivity data was obtained using the Fuch-Sondheimer- Mayadas-Shatzkes theoretical models (Steinhögl et al., J. Appl. Phys. 2005). Top Right: Schematic showing electron scattering at interfaces and grain boundaries in copper nanowires prepared using current damascene technology (from Steinhögl et al., Semiconductor International 2005).*

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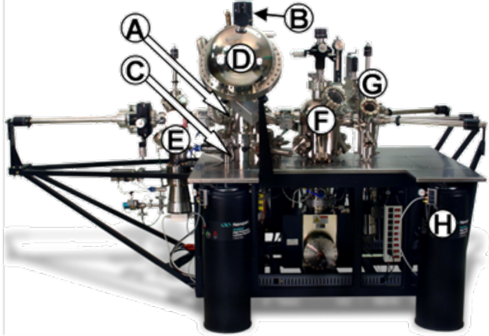
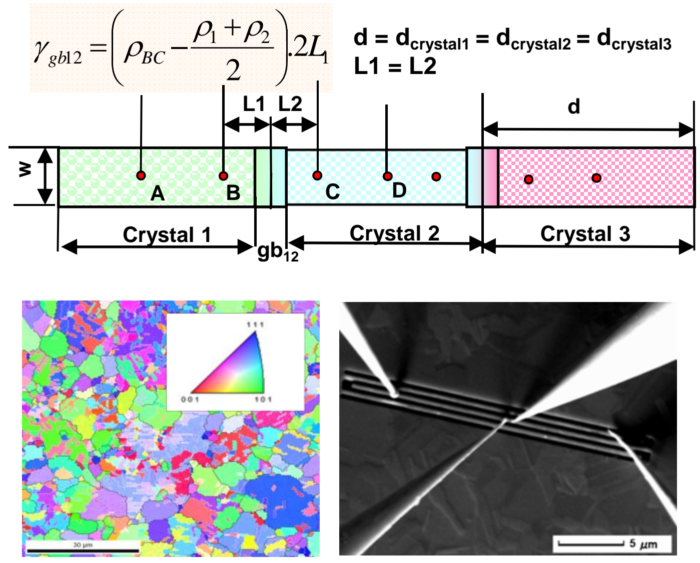
C. Copper Grain Boundary Resistivity Measurements with Four-Probe Scanning Tunneling Microscopy (STM): Large grained (microns) electroplated films of copper obtained from Intel were milled using a Dual-Beam Focused Ion Beam (FIB) system to obtain copper nanowires. Using a Four-probe STM at ORNL, the electrical resistance across various grain boundaries that spanned the width of the line was measured at two different temperatures. The temperature coefficient of resistance (TCR) technique was used to obtain the copper grain boundary resistivities from the measured resistances, and correlated with the corresponding grain boundary types using an electron backscatter diffraction (EBSD) system attached to a scanning electron microscope (SEM). Results indicated that the grain boundaries observed in damascene copper can have a substantial resistivity contribution to the overall resistivity, especially for small grain sizes in damascene copper.

Cryogenic Four-Probe Scanning Tunneling Microscopy (STM) System



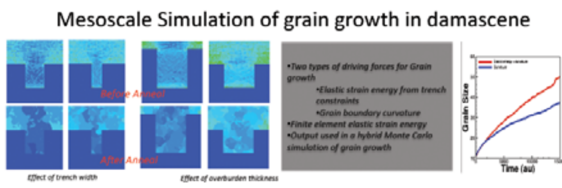
(A) Quadraprobe STM
(B) Electron gun for SEM
(C) Cryogenic Dewar for Liquid Helium
(D) Electron Energy Analyzer for SAM
(E) Probe Load-Lock Chamber
(F) MBE Chamber with RHEED
(G) Sample Load-Lock Chamber
(H) Air Legs for Vibration Isolation

Grain Boundary Resistance Measurements using the Four-Probe STM System at ORNL

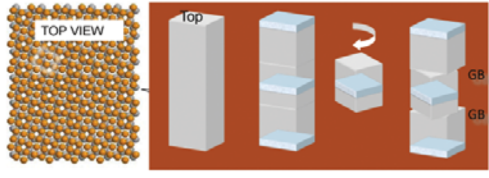


***Top Left:** Four Probe STM system at the Center for Nanophase Materials Science (CNMS), ORNL, which is used to conduct in situ nanoprobe resistance measurements. **Top Right:** Procedure for measuring the grain boundary resistivity by utilizing four-probe STM measurements of resistance across grain boundaries in copper electroplated film lines that were prepared using focused ion beam (FIB) milling. The grains in the copper film are represented by their orientations (colors) that were measured using orientation imaging microscopy (OIM) in a SEM system.*

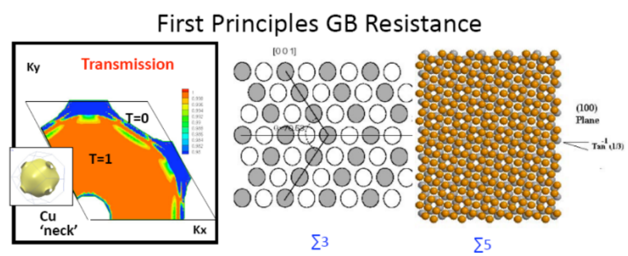
D. Modeling Interconnect Resistance and Microstructure: ORNL has formulated a modeling/validation approach to understand electron scattering in copper. This approach will use petascale computing to solve the electron transport problem in modeled microstructures containing grain boundaries and interfaces whose scattering properties are determined from first principles.



Multiple scattering theory (MST): electron transport



First Principles GB Resistance



Type of grain boundary	RA ($10^{-16}\Omega m^2$)	Relaxed or unrelaxed structure
Σ_3 (twin)	0.2	relaxed
Σ_3 (twin)	19.7	relaxed with Ga monolayer
Σ_5	0.6	unrelaxed
	1.9	relaxed
Σ_7	0.4	unrelaxed
Σ_{11}	0.9	unrelaxed

Twin Exp: 0.17 ($10^{-16}\Omega m^2$) Lei Lu Science 304, 422 (2004)

Proposed ARPA-E Project

- In the proposed work, plasma etching of copper blanket films will be carried out at sub-zero temperatures (< -40C) using a cryogenic ICP plasma etch tool at ORNL in order to obtain smooth, anisotropic nanoscale (<100 nm) copper features.
- In situ resistance measurements on the etched nanowires using the 4-probe STM at ORNL is expected to demonstrate the anticipated reduction (2X at 35 nm) in the electrical resistivity of copper CuRIE nanowires compared to copper damascene nanowires.
- A two-level copper interconnect including copper metal lines, vias, low-K dielectric and barriers will be demonstrated using CuRIE technology. E-beam lithography will be utilized for patterning in the first phase of the proposed work.
- Modeling and experimental efforts will be conducted to analyze the copper nanowire microstructure, resistivity, electromigration resistance, and other physical and mechanical properties of relevance.

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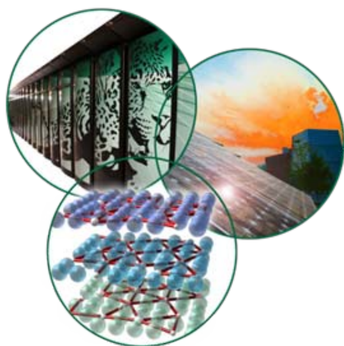

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